REMARKS/ARGUMENTS

By this paper, Applicant responds to the Office Action of January 13, 2005 and respectfully requests consideration of the application. A Petition for Extension of Time extends time to respond through June 13, 2005.

Claims 1-81 are now pending, a total of 81 claims. Claims 1, 2, 24, 34, 46, 52 and 70 are independent. The Office Action summary, stating that "claims 1-30 are pending," is wrong.

The amendments to the claims to recite "for storage in the memory of the computer" and "having a data structural form" and the like merely expressly recite limitations that were previously inherent in the claims. These amendments neither alter the scope of the claims nor respond to any statutory patentability concern.

I.   Claims 2-33

Claim 2 recites as follows:

> 2. A method, comprising:
>
> executing a program on a computer;
>
> recording in a memory of the computer profile information concerning the execution of the program, the profile information recording <u>the address of the last byte of at least one multi-byte instruction</u> executed by the computer during a profiled interval of the execution.

The Office Action asserts that the underlined language is "inherent" in Heisch '033.

As an initial matter, Applicant notes that the Office Action is incomplete, and is thus insufficient to raise any rejection over Heisch '033. Reliance on inherency is governed by MPEP § 2112 (underline in MPEP):

> IV.   EXAMINER MUST PROVIDE RATIONALE OR EVIDENCE TENDING TO SHOW INHERENCY
>
> The fact that a certain result or characteristic <u>may</u> occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic....
>
> "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic <u>necessarily</u> flows from the teachings of the applied prior art." ... The Board reversed on the basis that the examiner did not provide objective evidence or cogent technical reasoning to support the conclusion of inherency.).

Here, the Office Action merely asserts that "annotating" is inherent, without any "basis in fact or technical reasoning" to support the assertion. Without any "objective evidence or cogent technical reasoning," no rejection exists, and Applicant is unable to respond directly.

Nonetheless, in order to advance prosecution, Applicant offers the following observation. There is no reason to believe that Heisch '033 records "the address of the last byte." Conventional profiling systems record program counter values, which indicate the address of the first byte of instructions profiled. The Office Action indicates no reason to believe that Heisch departs from this conventional practice, let alone "necessarily" does so.

Claims 1 and 24 recite similar language, and are likewise not rejected, and are patentable over Heisch '033. The claims dependent thereon, 3-23 and 25-33, are similarly not rejected.

II.   Claims 34 and 46

Claim 34 recites as follows:

> 34.   A method, comprising:
>
> executing a program on a computer, without the program having been compiled for profiled execution, the program being coded in an instruction set in which an interpretation of an instruction depends on a processor mode not expressed in the binary representation of the instruction;
>
> recording in a memory of the computer profile information describing an interval of the program's execution and processor mode during the profiled interval of the program, the profile information having a data structural form efficiently tailored to annotate the profiled binary code with sufficient processor mode information to resolve mode-dependency in the binary coding.

The second underlined portion of claim 34 is entirely absent from the Office Action – it is simply reduced to an ellipsis with no explanation. Further, the right column of paragraph 3 of the Office Action misquotes the claim: "processor mode" is recited as a limitation on the instruction set, not of the compilation. Without complete consideration of the entire claim as it is currently pending, claim 34 is not rejected.

Nonetheless, in order to advance prosecution, Applicant offers the following observation. The first underlined portion distinguishes Heisch '033. Heisch '033 teaches that he is using "trace directed" techniques, col. 2, lines 31-37 and col. 4, line 53. "Trace directed" is a term of art, originally coined by Joseph Fisher, "Trace Scheduling, A Technique for Global Microcode Compaction, IEEE Transactions on Computers C-30(7):478-490 (July 1981), and J. R. Ellis,

Bulldog: A <u>Compiler</u> for VLIW Architectures, Technical Report YALEU/DCS/RR-364, Yale University, Department of Computer Science, reprinted by the MIT Press (1985). As Ellis' title suggests, "trace directed" techniques are implemented in a <u>compiler</u>. *See also* Exhibit A hereto, Manvi Agarwal et al., "Speculative Trace Scheduling in VLIW Processors," International Conference on Computer Design (ICCD'02), Freiburg, Germany (September 16 - 18, 2002) (describing Ellis: "In trace scheduling, [a] <u>compiler</u> picks..."); K. D. Cooper and P. Schileke, Non-local instruction scheduling with limited code growth, in Proc. ACM SIGPLAN Workshop Languages, Compilation, and Tools Embedded Systems, 1998, pp. 193—207 ("The first automated global scheduling technique was <u>trace scheduling</u>, originally described by Fisher. The technique has been used successfully in several research and industrial <u>compilers</u>."); U.S. Pat. No. 4,833,599, col. 6, line 66 to col. 7 line 1 ("the <u>compiler</u> uses the Trace Scheduling method..."). The indicated portions of Heisch '033 contain nothing to suggest that Heisch does anything other than traditional "trace" profiling, using compilation for profiled execution, the opposite of what is recited claim 34 ("<u>without the program having been compiled for profiled execution</u>").

Claims 1 and 46 recite similar language, and are similarly not rejected. The claims dependent thereon, 35-45 and 47-55, are similarly not rejected.

III.   Claims 52 and 70

Claim 52 is copied to this application from 09/330,852, in order to reduce issue fees and maintenance fees payable on issuance. The '852 application will be abandoned on allowance of these claims. Claim 52 recites as follows:

> 52. A method, comprising:
>
> during a profiled interval of an execution of a program on a computer, recording profile information describing the execution, without the program having been compiled for profiled execution, the program being coded in an instruction set in which an interpretation of an instruction depends on a processor mode not expressed in the binary representation of the instruction, the recorded profile information describing at least all events occurring during the profiled execution interval of the two classes:
>
>> a divergence of execution from sequential execution;
>>
>> a processor mode change that is not inferable from the opcode of the instruction that induces the processor mode change taken together with a processor mode before the mode change instruction;

the profile information further identifying <u>each distinct physical page</u> of instruction text executed during the execution interval.

Profiling is traditionally performed entirely in the <u>virtual</u> address space of a computer, and the profiler is kept deliberately ignorant of "physical" addresses, as recited claim 52. The January Office Action in the '852 application points to nothing in Heisch to suggest that Heisch departs from this traditional practice. Heisch '033 <u>must</u> work with virtual addresses, not "physical" addresses, as recited in claim 1. For example, all of the program events he discusses – branches, basic blocks, tracebacks, function calls, etc. – operate on the basis of virtual addresses, not physical addresses. If Heisch tried to base his profiler on physical addresses, it wouldn't work – the profiler would be incompatible with everything else that works with virtual addresses, and the system would break any time part of a program was moved from one physical address to another by the virtual memory system.

Second, the Office Action is incomplete because it fails to make a proper showing of inherency. Any rejection based on inherency is governed by MPEP § 2112:

2112 Requirements of Rejection Based on Inherency; Burden of Proof

...

IV. EXAMINER MUST PROVIDE RATIONALE OR EVIDENCE TENDING TO SHOW INHERENCY

The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. ...

"In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic <u>necessarily</u> flows from the teachings of the applied prior art."

The Office Action makes the bald statement that Heisch '033 "inherently includes pages." The Office Action provides no "basis in fact and/or technical reasoning" to address the language recited in the claim, profile information "identifying each distinct physical page of instruction text executed." Because the Office Action is incomplete, no rejection exists.

Claim 70 recites similar language, and is patentable for similar reasons.

Claims 2-18 and 20-30 are dependent on claims 1 and 70, and allowable therewith. In addition, they recite other patentable features that further distinguish the art.

IV. Claim 1

Claim 1 recites a number of limitations on which the Office Action is simply silent. For example:

- profile circuitry configured to detect and record, without compiler assistance for execution profiling

- the computer including instruction pipeline circuitry configured to execute instructions of the computer

- profile circuitry configured to detect and record, without compiler assistance for execution profiling

- events that match time-independent selection criteria of profileable events to be profiled, configuring the profile circuitry to record no profile information in response to the occurrence of profileable events

- the triggering event being one of a predefined class of triggering events

- configuring the profile circuitry to commence a profiled execution interval

- record[ing] profile information describing every event during a profiled execution interval that matches the time-independent profileable event selection criteria induced during the profiled execution interval

- the recorded profile information being efficiently tailored ... to annotate the profiled binary code with sufficient processor mode information to resolve mode-dependency in the binary coding

- he recorded profile information ... indicating contiguous ranges of sequential instructions executed during a profiled interval by low and high boundaries of the contiguous ranges, indicating the high boundary by the address of the last byte of the range

- the profile information ... identifying each distinct physical page of instruction text executed during the execution interval

The MPEP nowhere authorizes wholesale redrafting of claims by an examiner, or discounting claim limitations – especially when those limitations are ignored without explanation. Indeed, the MPEP forbids the practice, by negating all possible exceptions:

- MPEP ¶§ 2131: "To Anticipate A Claim, The Reference Must Teach <u>Every</u> Element Of The Claim"

- MPEP § 2143.03: "Indefinite claim limitations must be considered. A claim limitation which is considered indefinite <u>cannot be disregarded</u>."

- MPEP § 2173.05(g): "<u>A functional limitation must be evaluated and considered</u>, just like any other limitation of the claim..."

- MPEP § 2173.06: "<u>All words in a claim</u> must be considered in judging the patentability of a claim against the prior art."

- MPEP § 2106(VI), 2112.01(III): printed matter that is "functionally related" to the substrate must be considered for patentability (*citing In re Gulack*, 703 F.2d 1381, 1385-86, 217 USPQ 401, 404 (Fed. Cir. 1983). "'Functional descriptive material' consists of data structures and computer programs which impart functionality <u>when encoded on a computer-readable medium.</u>" MPEP § 2106(IV.B.1); *Ex parte Peppel*, http://www.uspto.gov/web/offices/ dcom/bpai/decisions/fd982848.pdf, 1998 WL 1766687 at *3 (BPAI 1998) (quoting MPEP).

The Office Action fails to meet the minimum requirements for stating a rejection of claim 1. No rejection of claim 1 exists.

V.   Claims 4, 6, 37 and 45

Paragraph 5 of the Office Action states that a given feature "is considered a choice of design." MPEP §§ 2143-2143.03 clarifies that this is not a permissible basis on which to consider obviousness. Rather, any obviousness rejection must make showings of "motivation to modify or combine," "reasonable expectation of success," and "all claim limitations taught or suggested." No obviousness rejections are raised.

Further, paragraph 5 of the Office Action is silent on "reasonable expectation of success." MPEP §§ 2143 and 2143.02 set out the Director's instructions, that no obviousness rejection can be raised without some showing of "reasonable expectation of success."

These claims are not rejected.

VI.   Dependent claims

Dependent claims 3, 5, 7-36, 38-44, and 46-51 are patentable with the independent claims discussed above. In addition, the dependent claims recite additional features that further distinguish the art.

A number of the dependent claims recite limitations analogous to those noted above in connection with claim 1 in section IV. The Office Action is silent on these claim limitations. A claim that recites a limitation absent from the art is not rejected.

Piecemeal examination is discouraged by 37 C.F.R. § 1.105 and MPEP § 707.07(g). It is requested that any future Office Action indicate the allowability of any claim that recites a limitation against which no prior art is cited. Applicant also notes that any new ground of rejection will prevent final rejection.

VII. Conclusion

Applicant notes the exceptional carelessness exhibited in this Office Action. The Summary page indicates claims 1-30 were pending; that is wrong, claims 1-51 were pending. As noted above, most of the independent claims recite language that is simply ignored in the Office Action. No showings of inherency or obviousness are made. The "double patenting" discussion in the Office Action mixes up "same invention" type double patenting and "obviousness" type double patenting, using a made-up legal standard, without an element-by-element comparison of any claim to a claim of the '401 application, as required by the MPEP.

Applicant respectfully observes that this application has been pending for <u>over six years</u>. A proper first Office Action is long overdue. No rejection can be made final when no proper first Office Action has been issued. If the application is not allowed, Applicant respectfully requests a first Office Action that properly sets forth the Examiner's views in a way that allows a full and direct response.

In view of the amendments and remarks, Applicant respectfully submits that the claims are in condition for allowance. Applicant requests that the application be passed to issue in due course. The Examiner is urged to telephone Applicant's undersigned counsel at the number noted below if it will advance the prosecution of this application, or with any suggestion to resolve any condition that would impede allowance. In the event that any further extension of time is required, Applicant petitions for that extension of time required to make this response timely. Kindly charge any additional fee, or credit any surplus, to Deposit Account No. 23-2405, Order No. 114596-07-4014.

Respectfully submitted,

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Dated: <u>July 12, 2005</u>

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Exhibit A to

Response to Office Action